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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

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Page 1 of 1

PATENT NO. : 7,560,958 B1
APPLICATION NO. : 10/619169
DATED : July 14, 2009
INVENTOR(S) : Francisco Javier Guerrero Mercado

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

[REDACTED]

Delete the title page and substitute therefore the attached title page showing the corrected number of Drawing Sheets in patent.

Delete Drawing Sheets 1 - 4 and substitute therefore the attached Drawing Sheets 1 - 2 ~~respectively~~ ~~and~~

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]



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(12) United States Patent
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(45) Date of Patent: Jul. 14, 2009

(54) LOW POWER COMPARATOR WITH FAST PROPAGATION DELAY

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(73) Assignee: National Semiconductor Corporation, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1066 days.

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(22) Filed: Jul. 14, 2003

(51) Int. Cl.
H03K 5/22 (2006.01)(52) U.S. Cl. 327/58; 327/63; 327/65;
327/89(58) Field of Classification Search 327/52,
327/53, 54, 56, 58, 63, 65, 66, 67, 72, 77-79,
327/80, 81, 88, 89

See application file for complete search history.

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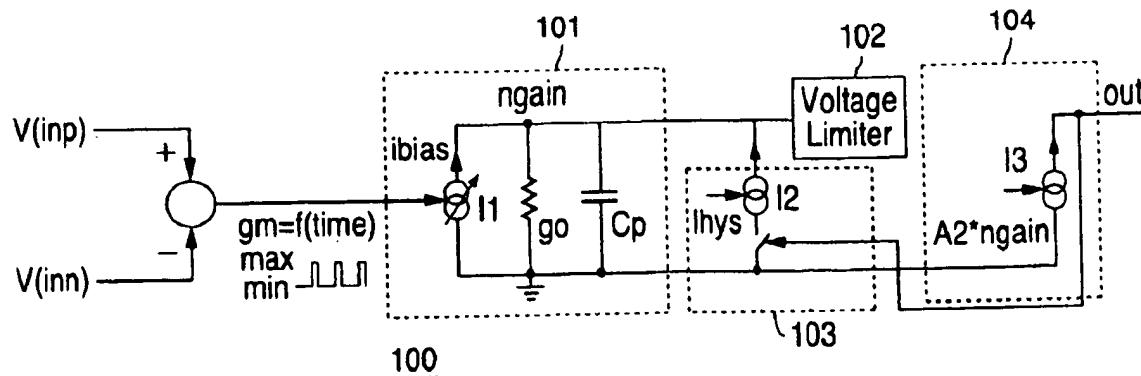
* cited by examiner

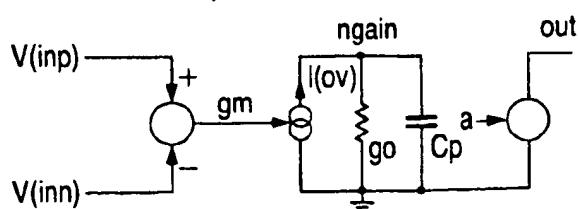
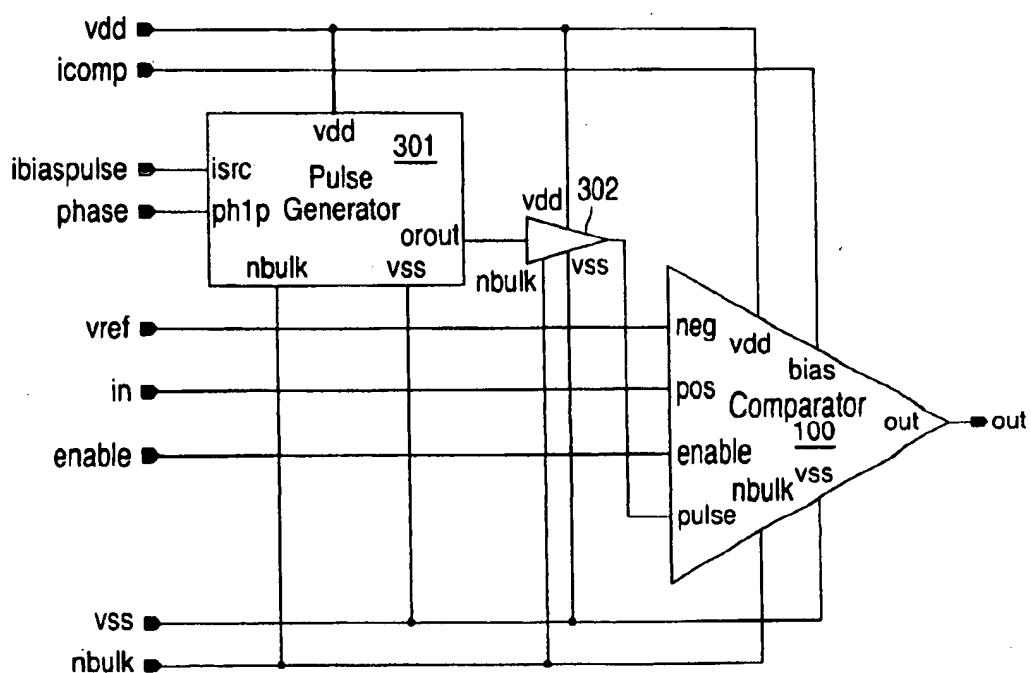
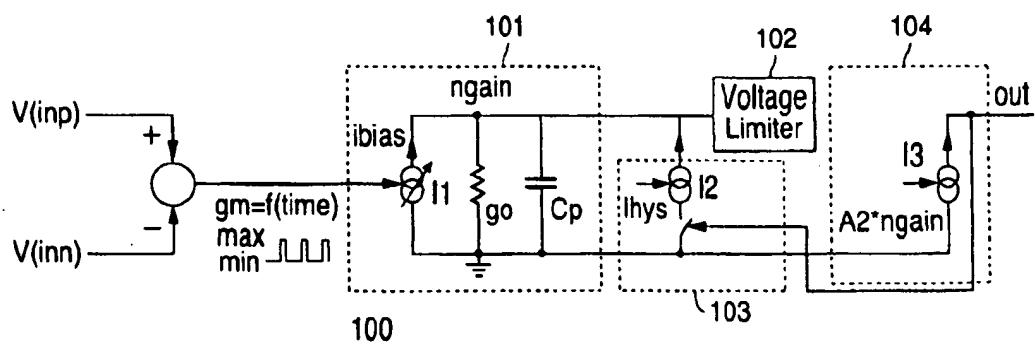
Primary Examiner—Tuan Lam

(57) ABSTRACT

A direct relationship exists between an integrated comparator's propagation delay and the input differential pair's bias current and overdrive voltage. A new method using a pulsed bias scheme for the input differential pair improves propagation delay by more than one order of magnitude without increasing significantly the average quiescent current, as long as the pulse width of the bias current is small relative to the system clock. A voltage limiter optimizes the comparator's transition time and a built-in hysteresis circuit minimizes spurious output transitions whenever the pulsed bias current pulse changes state. The bias current pulse and sampling of the comparator occur in predefined relation to the system clock.

20 Claims, 2 Drawing Sheets





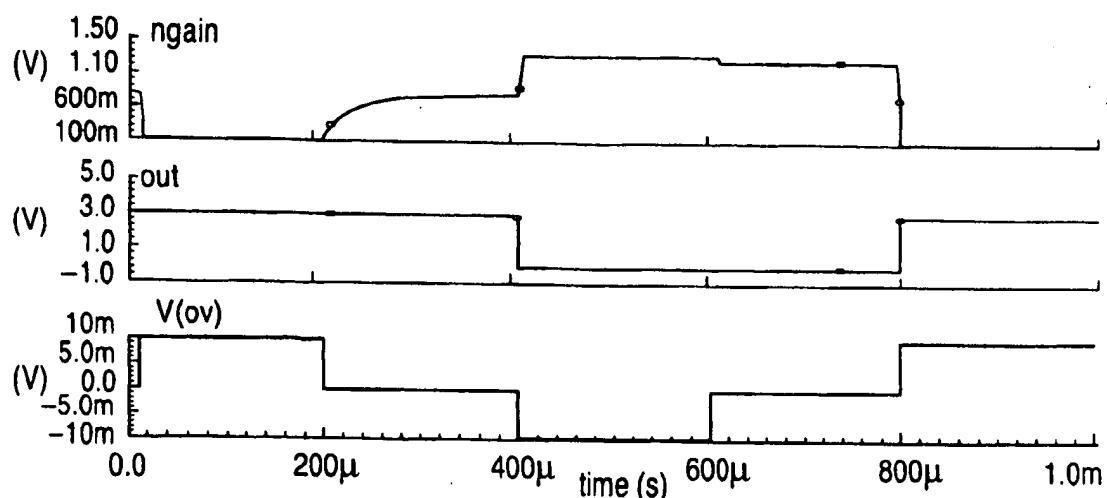


FIG. 2A

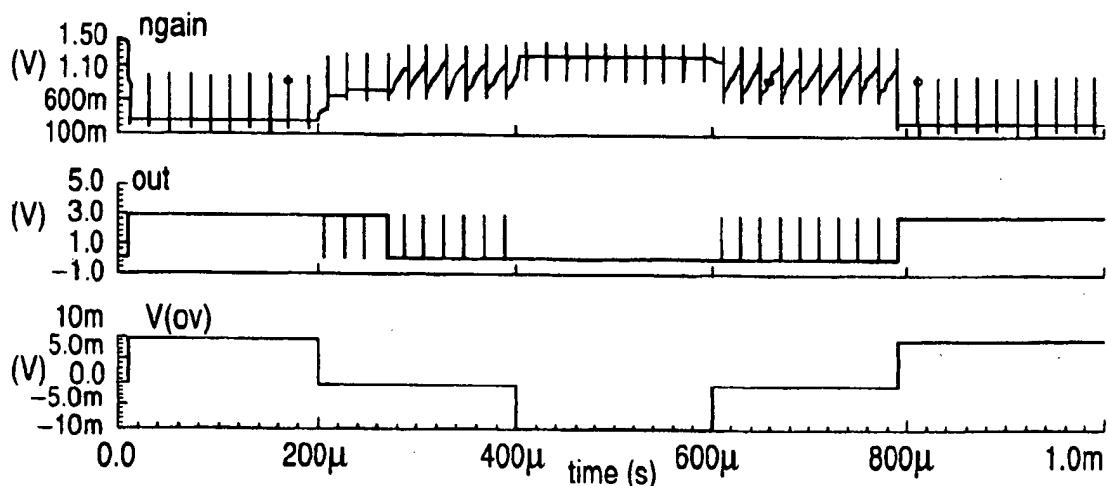


FIG. 2B

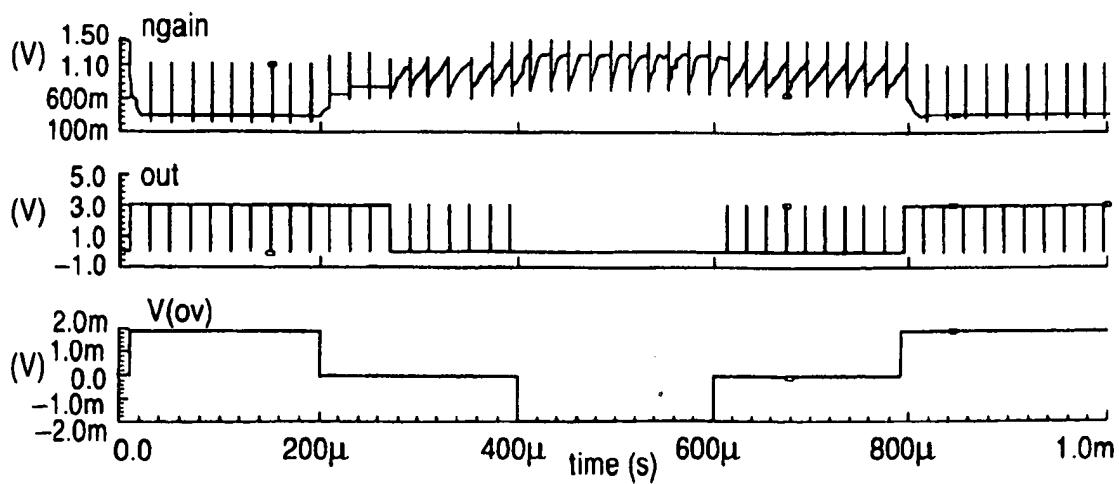


FIG. 2C